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10/713,729	11/13/2003	Bruce W. McGaughy	10585-016-999	2684
25226	7590	09/25/2006	EXAMINER	
MORRISON & FOERSTER LLP 755 PAGE MILL RD PALO ALTO, CA 94304-1018			SILVER, DAVID	
			ART UNIT	PAPER NUMBER
			2128	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/713,729

Applicant(s)

MCGAUGHY ET AL.

Examiner

David Silver

Art Unit

2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>6/21/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-24 are pending in Instant Application.

Information Disclosure Statement

2. The information disclosure statement(s) (IDS) submitted on 6/21/04 is/are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement(s) is/are being considered by the examiner.

Duty to Disclose / Requirement for Information

37 CFR 1.56 recites, in part:

"Each individual associated with the filing and prosecution of a patent application has a **duty of candor and good faith** in dealing with the Office, which includes a duty to **disclose to the Office all information known to that individual to be material to patentability** as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by § 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct."

3. It is noted that the Applicants have provided only the table of contents. Furthermore, it seems the book in its entirety may be deemed material to the patentability of the Instant Application. For example, Chapters 3, 4, 6, 8 of BSIM Pro+ Basic Operations appear to be directed to the invention the Applicant claims as his own. Furthermore, BSIM Pro Device Modeling Guide seems to be relevant **in its entirety** to the claimed invention.
4. The Examiner respectfully requests that the Applicants submit the documents listed on the IDS **in their entirety**. A 37 CFR 1.105 Requirement for Information is not currently made.
5. It is reasonable to take the position that the Applicants, who had access to the table of contents of the Celestry (currently part of Cadence Design Systems, inc), also had access to the books, in their entirety.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Art Unit: 2128

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-8, and 17-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

6.1 The method claims do not produce a useful, tangible, and concrete **result**. The steps of the method claims do not produce a useful, tangible, and concrete result. They merely recite a software algorithm, *per se*, which, for example, does not display, store, or otherwise provide a useful tangible output. Note exemplary claim 1 which only recites software steps and does not produce a useful tangible and concrete result. Although a simulation is claimed as the last limitations, there does not appear to be a **result** formed by the simulation.

6.2 As per claims 17-24, absent an explicit and deliberate definition in the specification that the product includes an appropriate medium or hardware elements, the claims are directed to software *per se*. Note exemplary claim 17 which recites only software elements. Additionally, software, *per se*, is not considered concrete under the above-recited MPEP citation (MPEP 2106). The claim recites a "medium"; however, the Specification does not unambiguously define that the medium is a tangible element.

6.3 Claims 9-16 are statutory for at least the following reasons: the system claims contains hardware elements (processing unit and display) and a result (viewing representations of the circuit on a display).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-24 are rejected on the ground of nonstatutory double patenting over claims 1-18 of **U. S.**

Patent No. 7,024,652 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

Instant Application	U.S. Patent No. 7,024,652
1. A method of simulating a circuit having a hierarchical data structure, comprising:	1. A method of simulating a circuit having a hierarchical data structure, comprising:
representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph;	representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph;
the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits;	the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits;
wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches;	wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches;
selecting a group of leaf circuits from the first and second branches for simulation;	selecting a group of leaf circuits from the first branch and the second branch for simulation, wherein each leaf circuit is represented by a matrix comprising a set of equations;

if two or more leaf circuits of the circuit having a substantially same isomorphic behavior, representing the two or more leaf circuits as a merged leaf circuit;	determining a strength of coupling between two or more leaf circuits of the group in accordance with a set of predetermined electrical coupling criteria;
creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit;	if two or more leaf circuits are deemed be strongly coupled, combining the corresponding matrix of each strongly coupled leaf circuit into a combined matrix;
wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits; and simulating the group of leaf circuits in accordance with the first port connectivity interface.	performing computation for the two or more strongly coupled leaf circuits in accordance with the combined matrix.

The table above is merely exemplary.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 2, 6, 10, 14, 18, and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the **enablement requirement**. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Art Unit: 2128

As per claims 2, 6, 10, 14, 18, and 22, the claims fail to comply with the enablement requirement because they do not enable "internal topologies, internal states and external loads are observed by the two or more leaf circuits". How can two or more leaf circuits "observe" the internal topologies, internal states and external loads? What is meant by "observe"?

9. Claims 9-16 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for **omitting essential structural cooperative relationships** of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: claim 9: the relationship between the processing unit, the computer programs, and the remainder of the claim.
10. Claims 2, 3, 5, 6, 7, 10, 11, 14, 17, 18, 19, 21, 22, 23 are rejected under 35 U.S.C. 112, second paragraph, as being **indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
11. The terms "substantially same" and "substantially different" in claims 2, 3, 5, 6, 7, 10, 11, 14, 17, 18, 19, 21, 22, 23 are relative terms which renders the claims indefinite. The terms "substantially same" and "substantially different" are not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
12. The above cited rejections are merely exemplary. The Applicant(s) are respectfully requested to correct all similar errors.
13. Claims not specifically mentioned are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Art Unit: 2128

14. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Tcherniaev (**US 6,577,992**).

Tcherniaev teaches: 1. A method of simulating a circuit having a hierarchical data structure, comprising:

representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph (**Fig 2A and text further expanding on the features**);

the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits (**Fig 2A and text further expanding on the features**);

wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches (**Fig 2A and text further expanding on the features**);

selecting a group of leaf circuits from the first and second branches for simulation (**Fig 2A items 206 & 208 and text further expanding on the features**);

if two or more leaf circuits of the circuit having a substantially same isomorphic behavior, representing the two or more leaf circuits as a merged leaf circuit (**col: 3 line: 56 to col: 4 line: 27**);

creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit (**col: 4 line: 44-47; Fig 2B; Fig 2C-2D; Fig 3 items 306 and 308; and text which further expands on the figures features**);

wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits (**col: 4 line: 44-47; Fig 2B; Fig 2C-2D; Fig 3 items 306 and 308; and text which further expands on the figures features**); and

simulating the group of leaf circuits in accordance with the first port connectivity interface (**col: 4 line: 44-47; col: 4 line: 53-59; Fig 2B; Fig 2C-2D; Fig 3 items 306 and 308; and text which further expands on the figures features**).

Art Unit: 2128

Tcherniaev teaches: 2. The method of claim 1, wherein the substantially same isomorphic behavior comprises:

a substantially same set of input signals are received by the two or more leaf circuits (**Fig 4 and texts further expanding on the features**);

a substantially same set of internal topologies, internal states, and external loads are observed by the two or more leaf circuits (**col: 3 line: 40-44; col: 3 line: 56 to col: 4 line: 27**); and

a substantially same set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals (**col: 3 line: 56 to col: 4 line: 27**).

Tcherniaev teaches: 3. The method of claim 1, wherein the substantially same isomorphic behavior is monitored at the output ports of the leaf circuits and at the first port connectivity interface of the group of leaf circuits (**col: 3 line: 56 to col: 4 line: 27**).

Tcherniaev teaches: 4. The method of claim 1, wherein the first port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of one or more receiver leaf circuits; a set of output vectors for referencing to a set of output ports of one or more driver leaf circuits; a set of load vectors for referencing to a set of loads of the one or more driver leaf circuits; and an array of storage elements for storing information associating the set of loads to the set of input ports (**Fig 2A, Fig 2B, Fig 2D (item 260 Elements Connectivity Model Parameter / Fanin/Fanout list / Port connectivity), Fig 3 item 304, Fig 2E and texts which further expand on the figures features**).

Tcherniaev teaches: 5. The method of claim 1, further comprising:

if the two or more leaf circuits represented by the merged leaf circuit demonstrating substantially different isomorphic behaviors, splitting the merged leaf circuits into two or more individual leaf circuits (**Fig 4 item 410 "Coupling strength"; Fig 8 item 726; Fig 9 item 818; Fig 10 item 1012; and texts which further expand on the figures features**);

creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits (**Fig 4 item 414; Fig 8 item 726; Fig 9**

Art Unit: 2128

item 818; Fig 10 item 1012; and texts which further expand on the figures features);
wherein the second port connectivity interface communicates changes in signal conditions among
the group of leaf circuits (**Fig 4 item 414; Fig 8 item 726; Fig 9 item 818; Fig 10 item**
1012; and texts which further expand on the figures features); and
simulating the group of leaf circuits in accordance with the second port connectivity interface
(Fig 2A items 206 & 208 and text further expanding on the features).

Tcherniaev teaches: 6. The method of claim 5, wherein substantially different isomorphic behaviors
include one or more elements selected from the group consisting of:

a substantially different set of input signals are received by the two or more leaf circuits (**Fig 4**
item 414; Fig 8 item 726; Fig 9 item 818; Fig 10 item 1012; and texts which further
expand on the figures features and texts further expanding on the features);
a substantially different set of internal topologies, internal states and external loads are observed
by the two or more leaf circuits (**Fig 4 item 410 "Coupling strength"; Fig 8 item 726; Fig 9**
item 818; Fig 10 item 1012; and texts which further expand on the figures features;
col: 3 line: 40-44; col: 3 line: 56 to col: 4 line: 27); and
a substantially different set of output signals are produced within a predetermined threshold of
signal tolerance by the two or more leaf circuits in response to a substantially same set of input
signals (**Fig 4 item 410 "Coupling strength"; Fig 8 item 726; Fig 9 item 818; Fig 10**
item 1012; and texts which further expand on the figures features; col: 3 line: 56 to
col: 4 line: 27).

Tcherniaev teaches: 7. The method of claim 5, wherein the substantially different isomorphic behaviors
are monitored at the output ports of the leaf circuits and at the second port connectivity interface of the
group (**col: 3 line: 56 to col: 4 line: 27).**

As per claim 8, note the rejection of claim 4 above. The Instant Claim is rejected under same prior-art
teachings.

As per claims 9-14, note the rejection of claims 1-8 above. The Instant Claims are functionally equivalent

Art Unit: 2128

to the above-rejected claims and therefore rejected under same prior-art teachings but for user interface **(col: 11 line: 57-59)**, memory **(col: 26 line: 46-55)**, netlist **(col: 3 line: 5-15)**.

As per claims 17-24, note the rejection of claims 9-14 above. The Instant Claims are functionally equivalent to the above-rejected claims and therefore rejected under same prior-art teachings.

Examiner Requests

15. The Examiner respectfully requests, in the event the Applicants choose to amend or add new claims, that such **claims and their limitations be directly mapped to the specification, which provides support for the subject matter**. This will assist in expediting compact prosecution.

Conclusion

16. All claims are rejected.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Silver whose telephone number is (571) 272-8634. The examiner can normally be reached on Monday thru Friday, 10am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Silver
Patent Examiner
Art Unit 2128

[Handwritten Signature]
KATH JONES P.H.D.
PRIMARY PATENT EXAMINER
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